

ACKNOWLEDGEMENT RECEIPT

Electronic Version

Stylesheet Version v01

**Title of
Invention**

**SELF-ALIGNED DRAIN/CHANNEL JUNCTION IN VERTICAL PASS
TRANSISTOR DRAM CELL DESIGN FOR DEVICE SCALING**

Submission Type : Utility Patent Filing

Application Number:

10/604731



EFS ID:

45500

Server Response:

Confirmation Code	Message
ISVR1	Submission was successfully submitted - Even if Informational or Warning Messages appear below, please do not resubmit this application
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First Named Applicant: Geng Wang

Attorney Docket Number: FIS920030209US1

Timestamp: 2003-08-13 13:42:02 EDT

From: US

File Listing:

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application-body	application-body.dtd	49498	2003-08-13
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